positive threshold voltage, the negative threshold voltage of the combined device is about the same as the negative threshold voltage of the NLE. The value of the erase voltage V_{ERASEC} in a combined device can be expressed as:

$$V_{ERASEC} \cong large\left(\frac{R_{MON}+R_{NON}}{R_{MON}} V_{ERASE}, V_{TH2}\right)$$

The relationship between the negative threshold voltages of a discrete and combined device can be expressed as:

$$V_{THC2} = \frac{R_{MON}+R_{NOFF}}{R_{NOFF}} V_{TH2} \cong V_{TH2}$$

So that in most embodiments, $V_{THC2} \approx V_{TH2}$.

Various embodiments of a digital NLE can be made of many different materials. For example, a digital NLE can be a threshold device such as a film that experiences a field-driven metal-insulating (Mott) transition. Such materials are known in the art, and include VO_2 and doped semiconductors. Other threshold devices include material that experiences resistance switching due to electronic mechanisms observed in metal oxides and other amorphous films, or other volatile resistive switching devices such as devices based on anion or cation motion in oxides, oxide heterostructures, or amorphous films. A digital NLE can also be in the form of a breakdown element exhibiting soft breakdown behavior such as SiO_2, HfO_2, and other dielectrics. Examples of such breakdown elements are described in further detail by application Ser. No. 12/826,653, filed on Jun. 29, 2010, which is entitled "Rectification Element for Resistive Switching for Non-volatile Memory Device and Method," and is incorporated by reference in its entirety. This reference discloses that additional materials may be used for a switching medium, for a NLE, for electrodes, and the like. In light of that disclosure, embodiments of the present invention may have a switching medium that includes: metal oxides such as ZnO, WO3, TiOx, NiO, CuO, or chalcogenide glass, organic materials, polymeric materials (inorganic or organic), and others. Additionally, in light of this disclosure, embodiments of the present invention may have an NLE that includes: an oxide dielectric material such as HfO2, a dielectric material or a combination of dielectric materials. Further, in light of this disclosure, the electrodes may be a metal or an alloy.

As is known in the art, the precise values of threshold, hold, program and erase can be adjusted for different embodiments by changing the form of and materials used for the NLE and the memory cell. In various embodiments the threshold voltage for the NLE can be about the same as the hold voltage, the program voltage, or both. In other embodiments the threshold voltage for the NLE can exceed the program and erase voltages of a resistive switching device.

An analog NLE differs from a digital NLE in that its I-V relationship is characterized by a more gradual transition when current starts to flow through the element. As shown in FIG. **7**A, which illustrates the response of an analog NLE to a voltage sweep, the current transition follows an exponential-like curve. The transition or threshold is therefore less abrupt than a digital NLE. Threshold voltage values where substantial current starts to flow through an analog NLE are designated as V_A and V_B for positive and negative bias values, respectively. Another significant difference between an analog and digital NLE is that an analog NLE does not experience the hysteretic hold voltage characteristic of a digital NLE.

FIGS. **7**B to **7**E show I-V characteristics of a combined device with an analog NLE. As shown in FIG. **7**B, when a program voltage $V_{PROGRAMC}$ is applied to a combined device where the switch is initially in an OFF state, the switch changes to a low resistance ON state. The $V_{PROGRAMC}$ is approximately the sum of the V_A of the NLE and the $V_{PROGRAM}$ of the switch as shown in FIG. **2**, or $V_{PROGRAMC} \approx V_A + V_{PROGRAM}$. As a result, the programming voltage of a combined device with an analog NLE is typically higher than the programming voltage of a switching element alone.

Turning now to FIG. **7**C, a negative voltage sweep of a combined device in an OFF state is shown. Because the switch is already in an OFF state, the negative voltage does not induce a state change, and the switch remains in a high resistance state.

FIG. **7**D shows the result of a read operation in a combined switch that is in an ON state. In the present embodiment, $V_{AC} < V_{READ} < V_{PROGRAMC}$. Because the switch is already in a low-resistance ON state, current flow above the threshold voltage V_{AC} is characterized by low resistance. Circuitry can detect the current flow, resulting in a positive read result. The value for V_A is not affected by the switching apparatus in most embodiments, so typically $V_{AC} \approx V_A$.

FIG. **7**E shows an I-V curve for an erase operation in a combined device. To change the switch from the ON state to the OFF state, a voltage of V_{ERASEC} is applied to the combined device, thereby increasing the resistance of the switch. The voltage required to complete an erase operation in a combined device is normally the sum of the erase value of the discrete switch and the threshold value of the analog NLE, or $V_{ERASEC} \approx V_{ERASE} + V_B$.

An analog NLE can be any element that exhibits the above described behavior. Examples of suitable materials include a punch-through diode, a Zener diode, an impact ionization (or avalanche) element, and a tunneling element such as a tunneling barrier layer. Such elements can be fabricated using standard fabrication techniques.

In most embodiments, $|V_A, V_B| < |V_{PROGRAM}, V_{ERASE}|$. As is known in the art, the precise threshold values of V_A, V_B, program, and erase can be adjusted for different embodiments by changing the form of and materials used for the NLE and the memory cell. In various embodiments the threshold voltage for the NLE can be about the same as the program voltage. In other embodiments the threshold voltage can exceed the program and erase voltages.

In other embodiments, a resistive switching cell may be configured to retain multiple resistive states. That is, rather than being configured to have binary states of ON and OFF, a cell can retain a plurality of resistance states. An array of such switches has the same limitations regarding leakage current, and would similarly benefit from the inclusion of an NLE.

The examples and embodiments described herein are for illustrative purposes only and are not intended to be limiting. Various modifications or alternatives in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims.

What is claimed is:

1. A method for a semiconductor device having a plurality of memory devices formed between intersections of a first plurality of electrodes and a second plurality of electrodes, the method comprising: